

## **REMARKS/ARGUMENTS**

The present Amendment is responsive to the final Office Action mailed January 21, 2009 in the above-identified application.

Claim 6 is canceled without prejudice or disclaimer. Therefore, claims 1-5 and 7-20 are the claims currently pending in the present application.

Claim 1 is amended to incorporate a recitation previously recited by claim 6 (now canceled). Further, claim 8 is amended to depend from a claim still pending in the present application. Thus, the amendments to the claims add no new features. All features currently recited in the claims were recited in the previous Amendment. Accordingly, the amendments to the claims raise no issues that would require further searching and a Request for Continued Examination is not filed at this time.

### ***Rejection of Claims 1-5 and 9-15 under 35 U.S.C. §103***

Claims 1-5 and 9-15 are rejected under 35 U.S.C. §103 as being obvious over Ban, U.S. Patent No. 5,404,485 in view of Higuchi et al., U.S. Patent Application Publication No. 2002/0120820. Reconsideration of this rejection is respectfully requested.

Claim 1 requires a portable data storage device operable to write data with reference to a memory address mapping table configured to associate logical address regions with physical address regions, the portable data storage device including a master control unit operable, when the result of the first determination is negative, to modify the memory address mapping table in accordance with a block queue listing one or more queuing physical address regions to thereby associate a second physical address with the logical address, the second physical address belonging to a queuing physical address region at a head of the block queue, and following said modification of the memory address mapping table, the block queue is modified to place the first physical address at the rear of the block queue.

The Office Action acknowledges that Ban and Higuchi do not disclose that the first physical address is placed at the rear of the block queue, as now required by claim 1. Accordingly, even taken together in combination, Ban and Higuchi do not disclose or suggest the recitations of claim 1.

Claims 2-5 and 9-15 depend from claim 1 and are therefore patentably distinguishable over the cited art for at least the same reasons.

### ***Rejection of Claims 6-8 under 35 U.S.C. §103***

Claims 6-8 are rejected under 35 U.S.C. §103 as being obvious over Ban in view of Higuchi and further in view of Crawford et al., U.S. Patent No. 5,918,055. Reconsideration of this rejection is respectfully requested.

Without intending to limit the scope of the claims, an effect or an advantage according to an aspect of Applicant's invention as claimed in claim 1 is that an ordering of the queuing physical address regions is provided and this queuing physical address region may vary dynamically during real-time operation. For example, as explained further at Specification, page 16, lines 6-17 of the published international application of the present application, the original physical address region block 10 with a certain page that is not in the "erased" state is subsequently placed at the rear of the block queue, and then is reused at the third to the last time that the master control unit is instructed to write data to a non-erased page of the block. Thus, the block queue is modified and the first physical address is placed at the rear of the block queue. In fact, this ordering of the queuing physical address regions is already implicit in claim 1 even in its unamended form, because the physical address region at the head of the block queue is used to replace the original physical address region having an "unerased" physical address, and consequently the present amendment to claim 1 merely clarifies this feature.

Claim 1 requires a portable data storage device operable to write data with reference to a memory address mapping table configured to associate logical address regions with physical address regions, the portable data storage device including a master control unit operable, when the result of the first determination is negative, to modify the memory address mapping table in accordance with a block queue listing one or more queuing physical address regions to thereby associate a second physical address with the logical address, the second physical address belonging to a queuing physical address region at a head of the block queue, and following said modification of the memory address mapping table, the block queue is modified to place the first physical address at the rear of the block queue.

Ban discloses a unit allocation table that stores the status ("written", "deleted", or "free") of the physical addresses corresponding to each of the logical addresses of the flash file system.

Ban does not disclose or suggest that following said modification of the memory address mapping table, the block queue is modified to place the first physical address at the rear of the block queue. More generally, Ban does not disclose or suggest any ordering of the "free" physical addresses in the unit allocation table. Accordingly, Ban's device would have to scan

sequentially the unit allocation table to identify and to locate the “free” physical addresses, but could not locate the “free” physical addresses directly at the head of block queue. Consequently, the device of Ban would have to undertake a less convenient and more time and resource consuming sequential scanning to identify and locate the “free” physical address.

Further, claim 1 requires that the second physical address region is a queuing physical address region at the head of a block queue. Ban does not disclose or suggest any such feature, and thus does not disclose or suggest the block queue feature above-recited of claim 1.

Higuchi discloses a memory device for controlling nonvolatile and volatile memories that may be random-accessed and a controller that transfers data between the nonvolatile memory and the volatile memory (Higuchi, Abstract). Higuchi discloses a NAND flash memory (Higuchi, paragraph 7). Higuchi does not cure the above-discussed deficiencies of Ban and Crawford as they relate to the above-cited features of claim 1.

Crawford discloses managing digital resources, by reserving token values for certain digital resources in the digital system, such that a selected token value in a free-buffer-queue is then matched to an incoming digital resource request and then moved to a valid-request-queue (Crawford, Abstract). Thus, Crawford discloses that tokens are transferred between a free-buffer-queue and a valid-request-queue. Such tokens have little to do with the queuing physical address regions of the block queue recited in claim 1. Accordingly, even taken together in combination, Ban, Higuchi and Crawford do not disclose or suggest the recitations of claim 1.

Moreover, it is respectfully submitted that there would have been no motivation or suggestion for arriving at the proposed combination based on the cited references. As discussed, Ban discloses storing the status of the physical address corresponding to each of the logical addresses, while Crawford discloses tokens of the free-buffer-queue transferred to the valid-request-queue. Such solutions are mutually incompatible and there would have been no suggestion or motivation for combining them for arrive at the proposed combination. The Office Action appears to be engaging in impermissible hindsight reconstruction based on Applicant’s own disclosure by combining aspects of the disclosure of Ban and Crawford’s token-based solution. Accordingly, it is respectfully submitted that Applicant’s invention as claimed in claim 1 would not have been obvious based on the cited art.

Claims 7 and 8 depend from claim 1 and are therefore patentably distinguishable over the cited art for at least the same reasons. Claim 6 is canceled without prejudice or disclaimer and therefore the rejection is moot as to this claim.

***Rejection of Claims 17-20 under 35 U.S.C. §103***

Claims 17-20 are rejected under 35 U.S.C. §103 as being obvious over Ban in view of Higuchi and further in view of Horn et al., U.S. Patent Application Publication No. 2005/0050273. Reconsideration of this rejection is respectfully requested.

Horn does not cure the above-discussed deficiencies of Ban, Higuchi and Crawford as they relate to the above-cited features of claim 1. Further, the Office Action does not allege that Horn discloses or suggests such features. Accordingly, even taken together in combination, Ban, Higuchi and Horn do not disclose or suggest the recitations of claim 1.

Claim 17-20 depend from claim 1 and are therefore patentably distinguishable over the cited art for at least the same reasons.

In view of the foregoing discussion, withdrawal of the rejections and allowance of the claims of the application are respectfully requested.

THIS CORRESPONDENCE IS BEING  
SUBMITTED ELECTRONICALLY  
THROUGH THE UNITED STATES  
PATENT AND TRADEMARK OFFICE  
EFS FILING SYSTEM  
ON April 21, 2009

RCF:GB/jl

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